

**CUSTOMER NO.: 24498****Serial No. 09/869,397**

Reply to Final Office Action dated: 1/03/07

Response dated: 4/11/07

**PATENT****PF980092****REMARKS**

In the Office Action, the Examiner noted that claims 1-10 are pending in the application and that claims 1-10 stand rejected. By this response, all claims continue unamended.

In view of the following discussion, the Applicant respectfully submits that none of the claims are anticipated under the provisions of 35 U.S.C. § 102 or rendered obvious under the provisions of 35 U.S.C. § 103. Thus the Applicant believes that all of these claims and the application are now in allowable form.

**Rejections****A. 35 U.S.C. § 102**

The Examiner rejected claims 1-2, 5 and 7-10 under 35 U.S.C. § 102(e) as being anticipated by Isaka (U.S. Patent No. 5,706,388). The rejection is respectfully traversed.

Regarding claim 1, the Examiner alleges that Isaka discloses a process for recording a digital video and audio data stream wherein recording being carried out on a medium organized in the form of logic blocks in series and comprising a recording and reading head including all of the aspects of the Applicant's invention. The Applicant respectfully disagrees.

"Anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim" (Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co., 730 F.2d 1452, 221 USPQ 481, 485 (Fed. Cir. 1983)). (emphasis added). The Applicant respectfully submits that Isaka fails to teach each and every element of at least the Applicant's claim 1, which specifically recites:

"A process for recording a digital video and audio data stream wherein recording being carried out on a medium organized in the form of logic blocks in series and comprising a recording and reading head, said process comprises the steps of:

recording data on said medium as a pattern of at least one recorded block immediately followed by at least one unrecorded block; and

following the triggering of the reading of the recorded data, alternately reading a continuous series of said previously recorded blocks

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and continuing the recording of data in said unrecorded blocks immediately following the blocks read.

The Applicant's claim 1 finds support throughout the specification. More specifically, Claim 1 is directed to a process for recording a digital video and audio data stream wherein recording being carried out on a medium (hard disk 201 on page 5, line 23) organized in the form of logic blocks in series and comprising a recording and reading head, the process including the steps of recording data in a pattern of at least one recorded block immediately followed by at least one unrecorded block (see figure 9a, page 18 lines 10-13) and following the triggering of the reading of the data, alternately reading a continuous series of previously recorded blocks and continuing the recording of data in the unrecorded blocks immediately following the blocks read (see page 18 lines 14-21).

In contrast to the invention of the Applicant, at least as claimed by the Applicant's independent claim 1, Isaka teaches (see column 4 lines 53-57) that "the data is recorded in consecutive areas on the recording medium 6a in the receiving order". Such teachings in Isaka are in direct contrast to at least the Applicant's claim 1 in which the data is recorded as a pattern of at least one recorded block immediately followed by at least one unrecorded block. Therefore the data is not recorded in the receiving order, as the blocks unrecorded are recorded later and are thus interlaced with data previously recorded.

In contrast to the invention of the Applicant, in Isaka, the data is not interlaced, this is also clearly mentioned on column 6 lines 6-24 of Isaka. That is, in Isaka the data is recorded in successive blocks. Nothing in Isaka indicates that the data is recorded in one block, then one block is left free, then another block is recorded and so on, as taught in the Applicant's Specification and claimed by at least the Applicant's claim 1. Instead, Isaka teaches in column 6 lines 13-15 that in block 1 is recorded the first predetermined amount of data and in block n is recorded the nth predetermined amount of data. This clearly teaches that in Isaka the data is stored without letting at least one free block unrecorded between two recorded blocks as taught and claimed by the Applicant.

More specifically, in one embodiment of the invention of the Applicant, a first predetermined amount of data is recorded in block 1, a second predetermined

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amount of data is recorded in block 3, and in block  $(2n-1)$  is recorded the  $n$ th predetermined amount of data. As such, in the invention of the Applicant one block of data is left free after recording one block of incoming data. In the case where one recorded block is followed immediately by more than one unrecorded block, the  $n$ th amount of data is stored not in block  $(2n-1)$  but in a block of greater number than  $2n-1$ .

In figure 3 of Isaka as pointed out by the Examiner, it is clearly taught that data is recorded in contiguous blocks, see blocks  $n$ ,  $n+1$ ,  $n+2$ . There is not one recorded block immediately followed by one unrecorded block as taught in the Applicant's Specification and claimed by at least the Applicant's claim 1. This is in direct contrast to the invention of the Applicant (i.e., see figures 9a and 9b of Applicant's invention where it is clearly shown that one recorded block is followed by at least one unrecorded block, the blocks being written one block over two or over three but not one block after the other without letting at least one free block between each recorded block).

Regarding the reproducing mode, Isaka teaches that the data is read on the recording medium and transferred either in buffer 10 or 11. Isaka further teaches in column 5 lines 24-35 that "at the same time the recording/reproducing head is returned to the last recording position to continue the recording operation for the data supplied from either of the reception buffer memories 1 and 2. When the predetermined amount of data is recorded on the recording medium 6a, the recording/reproducing head is again moved to the last reproducing position to reproduce the predetermined amount of data similarly to the above mentioned manner". Therefore, it is clear that in Isaka the recording/reproducing head moves from a reproducing position to a recording position, whereas in our invention, the recording/reproducing head does not need to move from the recording position to the reproducing position as data is read and recorded in contiguous (successive) blocks which therefore does not require moving the head from one position to a non-continuous position. As such, the invention of the Applicant has a clear and distinct advantage over the invention taught and claimed in Isaka.

Even further, the Applicant respectfully submits that the abstract of Isaka as cited by the Examiner also absolutely fails to teach each and every aspect of the

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Applicant's claim 1. More specifically, the Applicant does not agree that the abstract discloses a recording system where recording of information currently received can be performed while displaying of data previously recorded as taught and claimed by the Applicant. That is the Applicant submits that the abstract of Isaka does not teach, suggest or anticipate at least how the blocks are recorded and read on the recording medium as taught in the Applicant's Specification and as claimed in at least the Applicant's claim 1.

In addition, the Applicant reiterates his arguments of the previous response. More specifically, in contrast to the invention of the Applicant, at least as claimed by the Applicant's independent claim 1, Isaka describes a process for recording a digital video and audio data stream wherein recording is carried out on a medium (hard disk 36), organized in the form of logic blocks in series and comprising a recording and reading head (column 4 line 36), the process comprising the steps of storing first in a buffer memory (35) the data before transferring them to the main memory (36) and also, when reading data on the main memory (36), data is initially sent to the buffer memory (35). The invention proposes a useful arrangement of the buffer memory in order to make the data transfers with the main memory using an efficient manner. However, the arrangement is dedicated to the management of the buffer memories and not to the arrangement of the main memory.

More specifically, In Isaka, and specifically referring to Figure 2, Isaka describes a main memory, which can be in the form of a band disk arrangement (see column 3 line 57) and can be a hard-disk (see column 3 line 9). This main memory is interfaced to the management of this memory with a buffer memory comprising an input buffer 35a, an output buffer 35b and a free space between these two buffers. A micro-processor initiates the data transfer from the buffer 4 to the buffer memory 35. Input data in the buffer memory 35 is transferred to the main memory 36 as soon as it is convenient under the supervision of the microprocessor 34....(see column 3 lines 60-67)...the stored data in main memory 36 is in due course transferred to the buffer memory 35 under supervision of the microprocessor 34...(see column 4 lines 1-3). Isaka teaches the management of the data in the buffer memory and not the management of the data in the main

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memory. That is, in Isaka, the buffer is divided in two parts and the blocks are read in one part and written in the other part. However, it is not the main memory which is written one block out of two as taught in the Applicant's Specification and claimed by at least the Applicant's claim 1. The Examiner specifically alleges that P1 and P2 are blocks but the Applicant respectfully submits that in Isaka, P1 and P2 are blocks of the buffer memory and not blocks of the main memory. In Isaka, the main memory is written in a conventional way, or at least it is not the object of Isaka as nothing is said in Isaka about the main memory.

The buffer memory of Isaka represents one embodiment to avoid having a delay induced by the movement of the head, the data being firstly stored in the buffer memory, so the buffer memory acts as a cache memory. However, it is not the same solution which is taught in the Applicant's Specification and claimed by at least the Applicant's claim 1. In order to avoid having such an additional buffer (35), claim 1 proposes the characteristics of "recording the data in one block out of two starting from a first block, following the triggering of the reading of the data, alternately of reading a previously recorded block and of continuing the recording in the block following the block read". That is, the invention of the Applicant is directed at least in part to solving the deficiencies of the invention of Isaka which needs and teaches an additional buffer (35). As such, the Applicant respectfully submits that the invention of the Applicant, at least with respect to claim 1, is a totally different solution than the one proposed in Isaka as Isaka does not teach, suggest or anticipate recording data in one block out of two, wherein the recording is carried out on a medium organized in the form of logic blocks. That is, Isaka absolutely fails to teach, suggest or anticipate "recording data in one block out of two starting from a first block" where the blocks are blocks of a recording medium as taught in the Applicant's Specification and claimed by at least the Applicant's claim 1.

Instead, in Isaka there is a buffer separated in two areas that the Examiner considers as equivalent to the blocks of the recording medium of the Applicant's claim 1. However, in Isaka, there is only one block for recording and one block for reading and they are not blocks of the main memory 36 (medium organized in the form of logic blocks) as taught and claimed by the Applicant, but instead are

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portions of the buffer 35. As such, the Applicant respectfully submits that Isaka absolutely fails to teach, suggest or anticipate the invention of the Applicant, at least with respect to claim 1, where it is clear that the main memory (medium organized in the form of logic blocks) comprises several blocks and that during a write operation, data is written leaving a free space in the data block chain for subsequent recording, the free space being a block as taught in the Applicant's Specification and claimed by at least the Applicant's claim 1.

As such, the Applicant submits that this is clearly a structural difference between the claimed invention and the cited prior art of Isaka. That is, in Isaka, there is clearly a need for an external memory buffer, and in contrast, in the invention of the Applicant, there is no need for such a buffer due to the characteristics of claim 1. More specifically, in Isaka, it is the main memory which comprises a single reading and writing head and the blocks are not blocks of the main memory but blocks of the buffer located between the main memory 36 and the microprocessor. In contrast, in the invention of the Applicant, there is a main memory comprising a single reading and writing head and this main memory is separated into logic blocks. The Applicant's teachings describe the management of this main memory during recording of data using a new inventive method of block management avoiding the loss of time during the switch between read and write operations and without the need of an external buffer as disclosed in Isaka.

Therefore, the Applicant submits that for at least the reasons recited above, independent claim 1 is not anticipated by the teachings of Isaka and, as such, fully satisfies the requirements of 35 U.S.C. § 102 and is patentable thereunder.

Likewise, independent claim 7 recites similar relevant features as recited in the Applicant's independent claim 1. As such, the Applicant respectfully submits that for at least the reasons recited above independent claim 7 is also not anticipated by the teachings of Isaka and also fully satisfies the requirements of 35 U.S.C. § 102 and is patentable thereunder.

Furthermore, dependent claims 2, 5 and 8-10 depend either directly or indirectly from independent claims 1 and 7 and recite additional features therefor. As such and for at least the reasons set forth herein, the Applicant submits that dependent claims 2, 5 and 8-10 are also not anticipated by the teachings of Isaka.

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Therefore the Applicant submits that dependent claims 2, 5 and 8-10 also fully satisfy the requirements of 35 U.S.C. § 102 and are patentable thereunder.

**B. 35 U.S.C. § 103**

The Examiner rejected claims 3-4 under 35 U.S.C. § 103(a) as being unpatentable over Isaka in view of Official Notice. The rejection is respectfully traversed.

The Examiner applied Isaka for the rejection of claims 3-4 as applied above for the rejection of claims 1 and 7. As described above, Isaka absolutely fails to teach, suggest or anticipate at least the Applicant's independent claims 1 and 7. As such, and at least because Isaka fails to teach, suggest or anticipate the Applicant's independent claims 1 and 7, the Applicant further submits that Isaka also fails to teach, suggest or anticipate the Applicant's claims 3-4, which depend directly from the Applicant's claims 1 and 7, respectively.

As such and for at least the reasons recited above, the Applicant respectfully submits that the teachings of Isaka and Official Notice fail to teach, suggest or make obvious the invention of the Applicant with regard to at least the Applicant's independent claims 1 and 7. As such, the Applicant further submits that the teachings of Isaka and the Official Notice also fail to teach, suggest or make obvious the invention of the Applicant with regard to dependent claims 3 and 4, which depend directly from the Applicant's independent claim 1 and recite further limitations thereof.

Therefore, the Applicant submits that for at least the reasons recited above, the Applicant's claims 3 and 4 are not rendered obvious by the teachings of Isaka and the Official Notice and, as such, fully satisfy the requirements of 35 U.S.C. § 103 and are patentable thereunder.

**C. 35 U.S.C. § 103**

The Examiner rejected claim 6 under 35 U.S.C. § 103(a) as being unpatentable over Isaka in view of Ogawa (U.S. Patent No. 6,115,799). The rejection is respectfully traversed.

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The Examiner applied Isaka for the rejection of claim 6 as applied above for the rejection of claim 1. As described above, Isaka absolutely fails to teach, suggest or anticipate at least the Applicant's independent claim 1. As such, and at least because Isaka fails to teach, suggest or anticipate the Applicant's independent claim 1, the Applicant further submits that Isaka also fails to teach, suggest or anticipate the Applicant's claim 6, which depend directly from the Applicant's claim 1.

Furthermore, the Applicant submits that Ogawa also fails to teach, suggest or render obvious at least "recording data on said medium as a pattern of at least one recorded block immediately followed by at least one unrecorded block" and "following the triggering of the reading of the recorded data, alternately reading a continuous series of said previously recorded blocks and continuing the recording of data in said unrecorded blocks immediately following the blocks read" as taught in the Applicant's Specification and claimed by at least the Applicant's independent claim 1. That is, the teachings of Ogawa absolutely fail to bridge the substantial gap between the invention of Isaka and the invention of the Applicant.

More specifically Ogawa teaches an information processing apparatus, which can expand a part of a function by the addition of software. The invention of Ogawa enables the development of additional software that does not depend on the firmware version. The information processing apparatus of Ogawa manages a memory using, for example, a Next Fit method and may reduce memory fragmentation. A reduction in memory fragmentation may be performed before and after a photograph is taken in a camera using a flash memory, or before or after recording or erasing is performed. However, the Applicant submits that there is absolutely no teaching, suggestion or disclosure in Ogawa for a process for recording a digital video and audio data stream in which recording is being carried out on a medium organized in the form of logic blocks in series and including a recording and reading head where the process includes "recording data on said medium as a pattern of at least one recorded block immediately followed by at least one unrecorded block" and "following the triggering of the reading of the recorded data, alternately reading a continuous series of said previously recorded blocks and continuing the recording of data in said unrecorded blocks immediately



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following the blocks read" as taught in the Applicant's Specification and claimed by at least the Applicant's claim 1.

As such, the Applicant submits that at least because Ogawa fails to teach, suggest or render obvious at least the Applicant's independent claim 1, the Applicant further respectfully submits that Ogawa also fails to teach, suggest or render obvious the Applicant's claim 6, which depends directly from the Applicant's independent claim 1.

Furthermore, the Applicant submits that there is absolutely no motivation or suggestion in either reference for the combination of Isaka and Ogawa to attempt to teach the invention of the Applicant. More specifically, there is no motivation or suggestion in the invention of Ogawa for the combination of the references and likewise, the invention of Isaka does not expressly or impliedly motivate or suggest such a combination as required by for the combination of references under 35 U.S.C. § 103.

Even further, the Applicant submits that even if there was a motivation to combine the references (which the Applicant maintains that no such motivation exists), the teachings of Ogawa fail to bridge the substantial gap between the teachings of Isaka and the Applicant's invention at least with respect to independent claim 1 and as such dependent claim 6.

As such and for at least the reasons recited above, the Applicant respectfully submits that the teachings of Isaka and Ogawa, alone or in any allowable combination, fail to teach, suggest or make obvious the invention of the Applicant with regard to at least the Applicant's independent claim 1. As such, the Applicant further submits that the teachings of Isaka and Ogawa, alone or in any allowable combination, also fail to teach, suggest or make obvious the invention of the Applicant with regard to dependent claim 6, which depends directly from the Applicant's independent claim 1, and recites further limitations thereof.

Therefore, the Applicant submits that for at least the reasons recited above, the Applicant's claim 6 is not rendered obvious by the teachings of Isaka and Ogawa, alone or in any allowable combination and, as such, fully satisfy the requirements of 35 U.S.C. § 103 and are patentable thereunder.

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**PATENT  
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The Applicant respectfully submits that none of the claims are anticipated under the provisions of 35 U.S.C. § 102 or rendered obvious under the provisions of 35 U.S.C. § 103. Consequently, the Applicant believes that all these claims are presently in condition for allowance. Accordingly, both reconsideration of this application and its swift passage to issue are earnestly solicited.

If however, the Examiner believes that there are any unresolved issues requiring adverse final action in any of the claims now pending in the application, or if the Examiner believes a telephone interview would expedite the prosecution of the subject application to completion, it is respectfully requested that the Examiner telephone the undersigned.

No fee is believed due. However, if a fee is due, please charge the additional fee to Deposit Account No. 07-0832.

Respectfully submitted,

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April 11, 2007